REMARKS

The present application is being filed as a continuation of application serial number 09/823,527, filed March 30, 2001, pursuant to 37 C.F.R. §1.53(b). The applicants respectfully request consideration of the present application as amended. As a result of this preliminary amendment, claims 4, 7, 11, 16, and 20 from the parent application have been canceled. Therefore, claims 1-3, 5, 6, 8-10, 12-15, and 17-19 are currently pending in the present application.

In the Office Action from January 20, 2004 in the parent application, the Examiner has rejected claims 1, 2, 6, and 9 of the parent application under 35 U.S.C. § 102(a) as being anticipated by Applicant's Admitted Prior Art (AAPA).

Applicants respectfully traverse the rejection. In contrast to a bit-level interleaving of the presently claimed invention, AAPA's algorithm is performed by manipulating entire source data streams until the source data streams are interleaved along their lengths. More specifically, AAPA's algorithm includes iteratively shifting the source data streams to predetermined positions in the source registers, combining the resulting intermediate data streams using temporary registers, and then placing the combined data streams in a destination register. Such manipulation of data streams results in the interleaving of source data stream bits. In particular, each iteration described above results in the interleaving of just one pair of bits from the two source data streams and requires the execution of 10 instructions (see Fig. 5, blocks 510-528). Moreover, in order to interleave all the bits along the whole length of the data streams, these 10 instructions must be repeated as many times as the number of bits in the source data stream. Thus, for 16-bit data streams, AAPA's algorithm results in 163 executed instructions (i.e., the first 3 instructions and the loop resulting in 10 instructions executed 16 times) (see Specification, p.11, lines 6-9, and Fig. 5)

and requires twice as many registers as the presently claimed invention. These additional registers are the two temporary registers and a register to store a loop counter information. Thus, the AAPA method achieves interleaving by manipulating the entire streams of data. In the presently claimed invention, in contrast, the interleaving operation is performed by manipulating individual bits of the source data streams, i.e., it is performed at a bit-level, as recited in claim 1:

A computerized method comprising:
identifying a first stream of data stored in first source register and a second stream of data stored in a second source register; and
performing a bit-level interleaving of the first stream of data and the second stream of data to generate a combined stream of data.

(emphasis added).

Therefore, applicants respectfully submit that claim 1 is not anticipated by AAPA under 35 U.S.C. §102 (a).

Dependent claims 2-5 include all features of claim 1 and further limit it. Therefore, for at least the same reasons as advanced above with respect to claim 1, dependent claims 2-5 are not anticipated by AAPA under 35 U.S.C. §102 (a).

Independent claims 6, 9, and 13 and their corresponding dependent claims 7, 8, 10-12, and 14-17 include language that is similar to the language of claim 1: a bit-level interleaving of the first stream of data and the second stream of data to generate a combined stream of data. Therefore, applicants respectfully submit that for at least the same reasons as advanced above with respect to claim 1 independent claims 6, 9, and 13 and their corresponding dependent claims 7, 8, 10-12, and 14-17 are not anticipated by AAPA under 35 U.S.C. §102 (a).

Rejections Under 35 U.S.C. § 103(a)

In the parent application, claims 5, 8, and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA, in view of Romano et at. (US.5, 586, 306).

Applicants respectfully traverse the rejection. As discussed above, AAPA does not teach or suggest bit-level interleaving as recited in claim 1.

Romano discloses integrated circuit servo system control for computer mass storage device with distributed control functionality to reduce transport delay. The integrated circuit controls an electromechanical functionality of a computer mass storage device, such as a magnetic disk drive incorporating a spindle motor for rotatably controlling a disk and an actuator for positioning a read/write head with respect to the disk, to read or write encoded data and to sense encoded servo data. Romano does not teach or suggest performing a bit-level interleaving of the first stream of data and the second stream of data to generate a combined stream of data, as recited in claim 1. Consequently, Romano lacks the same features of claim 1 that are missing from AAPA.

Since AAPA and Romano, taken alone or in combination, do not teach or suggest all elements of the present invention as claimed in claim 1, applicants respectfully submit that claim 1 is not obvious under 35 U.S.C. § 103(a) over AAPA in view of Romano.

Each of independent claims 6, 9, and 13 includes language that is similar to the language of claim 1: a bit-level interleaving of the first stream of data and the second stream of data to generate a combined stream of data.

Thus, Applicants respectfully submit that for at least the same reasons as set forth above with respect to claim 1, independent claims 6, 9 and 13 and their corresponding dependent claims 7, 8, 10-12, and 14-17 are not obvious under 35 U.S.C. § 103(a) over AAPA in view of Romano.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. Applicants believe that the above amendments and arguments put the present case into proper form for allowance, and such allowance is respectfully requested.

Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicant hereby requests such extension.

Respectfully submitted,

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Dated: February 4, 2004

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